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| EXAMINER | |
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| LEE, CHUN KUAN | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/725,663 | DANILAK ET AL. | |
| | Examiner | Art Unit | |
| | Chun-Kuan Lee | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6,8-12 and 14-21* is/are pending in the application.

4a) Of the above claim(s) *2-5,9-11 and 14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,8,12 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/18/2009 & 03/16/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

## RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 01/19/2010 have been fully considered but they are not persuasive. Currently, claims 7 and 13 are canceled; claims 2-5, 9-11 and 14-20 are withdrawn; and claims 1, 6, 8, 12 and 21 are pending for examination.

2. In response to applicant's arguments with regard to the independent claims 1, 8 and 21 rejected under 35 U.S.C. 103(a) that the fact the office action assembles a conglomeration of different references (i.e. AAPA, Chisholm, Wilcox and Winkler) to show aspects of the disk controller of the claimed invention indicates the non-obviousness of the claimed invention; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

3. In response to applicant's arguments with regard to the independent claims 1, 8 and 21 rejected under 35 U.S.C. 103(a) that assembling the above cited references to kludge together aspects of the claimed invention could only be done impermissibly by using the claims as a roadmap; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

4. In response to applicant's arguments with regard to the independent claims 1, 8 and 21 rejected under 35 U.S.C. 103(a) that the combination of the references (e.g. Chisholm, Wood and Davis) does not teach/suggest the claimed features: bypass register, the bypass register is memory mapped and implements aggregation of transaction information from a host CPU by using a memory mapped data transfer, bus master controller coupled to the disk I/O engine, the bypass register coupled to the bus master controller, an arbiter coupled to the bus master controller and the disk I/O engine, and a disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command from the processor because Chisholm does not teach/suggest using memory mapped data transfers, memory mapping, DMA transfers via memory mapped registers, or the like; Chisholm does not teach/suggest a bus master controller, a bypass register coupled to the bus master controller, an arbiter coupled to the bus master controller and the disk I/O engine; Chisholm does not teach/suggest any memory mapped registers or the use of such memory mapped register to transfer a disk I/O commands or the advantage of using memory mapped

bypass registers for transferring disk commands; and neither Wood nor Davis shows disk controller memory mapped bypass register or use of such memory mapped bypass register to transfer a disk I/O command as Wood teaches the transferring of a start command to an array of disk drives and Davis teaches a bridge component of a computer system; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The examiner is not fully clear regarding to applicant's arguments, because applicant's arguments seems to be directed towards the examiner's preceding office action which relied on the teaching of Chisholm, Wood and Davis; however, base on the examiner's limited understanding of applicant's above arguments, the prior art relied upon by the examiner in the current outstanding office action does teach the above claim feature as following:

Chisholm teaches: a bypass register (Chisholm, Fig. 3, ref. 203, 311) coupled to a disk controller (Chisholm, Fig. 3, ref. 201, 203, 209, 213, 311), wherein the bypass register is memory mapped (e.g. register having address information that is memory mapped to where command/data is stored in the host memory) and implements aggregation (e.g. aggregation via transfer to accumulate) of transaction information (e.g. command block with transaction information for data transferring) from a host CPU (Chisholm, Fig. 3, ref. 103) by using a memory mapped data transfer (e.g. memory

mapped data transfer corresponding to the transferring of the command blocks via memory mapping by command block address to the host memory) (Chisholm, col. 5, l. 1 to col. 6, l. 8), wherein the register (Chisholm, Fig. 3, ref. 311) is memory mapped as the register comprises the command block address received from the host CPU for transferring of the command/data blocks (Chisholm, Fig. 3, ref. 301) (e.g. transaction information) (Chisholm, col. 5, ll. 25-34), wherein the command block address is mapped to where the corresponding command/data block is located in the host memory (Chisholm, Fig. 3, ref. 107); a disk I/O engine (Chisholm, Fig. 3, ref. 209, 213) coupled to the disk controller (Chisholm, Fig. 3, ref. 201, 203, 209, 213, 311); and the disk I/O engine (Chisholm, Fig. 3, ref. 209, 213) is configured to cause a start up of the disk drive upon receiving a disk start up command (e.g. command transfer start signal) from the processor (Chisholm, Fig. 1, ref. 114; Fig. 2, ref. 115; col. 4, ll. 26-36 and col. 5, l. 1 to col. 6, l. 8), as the disk drive starts up after receiving the command transfer start signal. Additionally, Chisholm does teach the above memory mapped data transferring is associated with DMA transfer as the DMA state machines (Fig. 3, ref. 322, 324) are utilized (Chisholm, col. 1, l. 52 to col. 2, l. 8 and col. 5, l. 1 to col. 6, l. 8); and the advantage of using Chisholm's bypass register (Fig. 3, ref. 203, 311) is the increasing of data transferring throughput by reducing the command block transfer overhead (Chisholm, col. 2, ll. 20-50 and col. 5, ll. 55-58). Furthermore, it is to the examiner's understanding that the claimed feature "bypass register" implements the data transferring without writing into the prior art 8 bit register, wherein Chisholm's "bypass

register" are not the prior art 8 bit register, which is utilized for implementing the data transferring (Chisholm, col. 5, l. 1 to col. 6, l. 21).

Winkler teaches a system and a method comprising: a bus master controller coupled to the disk I/O engine (e.g. hard disk controller) [0013], by combination Winkler's bus master controller with Chisholm's disk controller's disk I/O engine, the bypass register which is coupled to the disk I/O engine is coupled to the bus master controller; and an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller [0013], as the inclusion of the arbitration function within the disk controller enables proper coordination of the data transferring for disk drive system.

5. In response to applicant's arguments with regard to the dependent claims 6 and 12 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claim features that the disk controller, with respect to reciting a CPB pointer buffer coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers to extend to a number of disk transactions scheduled for execution by the disk I/O engine, and the CPB pointer buffers are directly connected to the I/O engine for control in a manner independent of the arbiter; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because Chisholm and Winkler teach the bridge component wherein the disk controller further comprising a CPB pointer buffer (Chisholm, command address queue 309 of Fig. 3) coupled to the disk I/O engine for

dynamically appending a plurality of CPB pointers (e.g. addresses pointing to where the command block are stored) to extend to a number of disk transactions scheduled for execution by the disk I/O engine (e.g. as the number of command blocks are extended), and the CPB pointer buffers (Chisholm, Fig. 3, ref. 309) directly connected to the disk I/O engine (Chisholm, Fig. 3, ref. 209, 213) for control independent of the arbiter (Chisholm, col. 5, l. 1 to col. 6, l. 8 and Winkler, [0013]).

6. In response to applicant's arguments with regard to the new independent claim 21 rejected under 35 U.S.C. 103(a) that the combination of references does not teach the claimed feature a chain memory coupled to the disk I/O engine for buffering a plurality of CPBs to extend a number of disk transactions scheduled for execution by the disk I/O engine and the chain memory, and the chain memory's functionality is separate and distinct from the operation of bypass register; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because Chisholm teaches a chain memory (e.g. section of the memory 203 storing the command blocks 304 of Fig. 3, wherein the command blocks are chained together as the addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a plurality of CPBs (Fig. 3, ref. 304) to extend a number of disk transactions scheduled for execution by the disk I/O engine, wherein Chisholm's chain memory maintains/stores the plurality of command blocks (Fig. 3, ref. 304) and Chisholm's bypass register transfers the command blocks from the host side to the

peripheral side to be executed (i.e. Chisholm's chain memory and bypass register have separate and distinct functions) (col. 5, l. 1 to col. 6, l. 21).

Additionally, the examiner requests the applicant to clarify as to where in applicant's Specification or Drawings disclose that the chain memory and its functionality is separate and distinct from the operation of the bypass register.

## I. REJECTIONS BASED ON DOUBLE PATENTING

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 12/005,745 in view of Chisholm et al. (US Patent 5,968,143), Winkler et al. (US Pub:. 2004/0024948) and Wilcox (US Patent 6,185,634).

Copending Application No. 12/005,745 teaches a disk controller for implementing efficient disk I/O for a computer system, comprising:

a bus interface for interfacing with a processor and a system memory of the computer system (claim 1);

a disk I/O engine coupled to the bus interface (claim 1);

a device interface coupled to the disk I/O engine for interfacing the disk I/O engine with a disk drive, wherein the disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command from the processor, the disk I/O engine further configured to execute a disk transaction by processing the disk transaction information from the bypass register coupled to the disk I/O engine (claim 1).

Copending Application No. 12/005,745 does not teach the disk controller for implementing efficient disk I/O for the computer system, comprising:

a bus master controller coupled to the disk I/O engine;

a bypass register coupled to the bus master controller, wherein the bypass register is memory mapped and implements aggregation of disk transaction information from a host CPU by using a memory mapped data transfer;

an arbiter couple to the bus master controller and the disk I/O engine, to coordinate data transfers within the disk controller;

a chain memory coupled to the disk I/O engine for buffering a plurality of CPBs to extend a number of disk transactions scheduled for execution by the disk I/O engine; and

the start up command configured to hide a start latency of the disk drive.

Chisholm teaches a disk controller for implementing efficient disk I/O for a computer system, comprising:

a disk controller (Fig. 3, ref. 201, 203, 209, 213, 311) for executing disk transactions (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21), the disk controller further comprising:

a disk I/O engine (Fig. 3, ref. 209, 213) coupled to the bus interface (Fig. 3, ref. 109, 111) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine, wherein the bypass register is memory mapped and implements aggregation (e.g. aggregation via transfer to accumulate) of disk transaction information (e.g. command block with transaction information for data transferring) from a host CPU (Fig. 3, ref. 103) by using a memory mapped data transfer (e.g. memory mapped data transfer corresponding to the transferring of the command blocks via memory mapping by command block address to the host memory) (col. 5, l. 1 to col. 6, l. 21), wherein the register (Fig. 3, ref. 311) is memory mapped as the register comprises the command block address received from the host CPU for transferring of the command/data blocks (Fig. 3, ref. 301) (e.g. transaction information) (col. 5, ll. 25-34), wherein the command block address is mapped to where the corresponding command/data block is located in the host memory (Fig. 3, ref. 107) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21); and

a chain memory (e.g. section of the memory 203 storing the command blocks 304 of Fig. 3, wherein the memory section is the chain memory storing the chain of

command blocks as the addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a plurality of command blocks (Fig. 3, ref. 304) to extend a number of disk transactions scheduled for execution by the disk I/O engine (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21).

Winkler teaches a system and a method comprising:

a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) ([0013]), by combining the bus master controller with Copending Application No. 12/005,745 and Chisholm's bypass register and disk I/O engine, the resulting combination further teaches the bypass register which is coupled to the disk I/O engine is coupled to the bus master controller; and

an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller ([0013]), wherein the inclusion of the arbitration function into the disk controller would enable proper coordination of the data transferring for disk drive system such as RAID.

Wilcox teaches a system and a method comprising: causing the start up before completion of said start up, the start up command configured to hide a start latency of the disk drive (Fig. 7; col. 2, ll. 10-23; col. 3, ll. 40-62; col. 5, ll. 7-41; and col. 11, l. 38 to col. 12, l. 57), as the delay to for the start up of data transferring is hidden.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Chisholm's interfacing architecture, Winkler's bus master controller and arbitration, and Wilcox's start up into Copending Application No. 12/005,745's computer system for the benefit of increasing data transferring throughput

by reducing the command block transfer overhead (Chisholm, col. 2, ll. 20-50 and col. 5, ll. 55-58), increasing the operation speed, as well as improving reliability and the efficiency in the transferring of data (Winkler, [0017]), ad reducing latency in the transferring of data to the disk drive (Wilcox, col. 1, ll. 19-23 and col. 2, ll. 51-53) to obtain the invention as specified in claim 1.

8. Claim 8 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 12/005,745 in view of Chisholm et al. (US Patent 5,968,143), Winkler et al. (US Pub:. 2004/0024948) and Wilcox (US Patent 6,185,634).

Copending Application No. 12/005,745 teaches a bridge component for implementing efficient disk I/O for a computer system, comprising:

a bus interface for interfacing with a processor and a system memory of the computer system (claim 5);

a disk controller for executing disk I/O transactions for the computer system (claim 5), the disk controller further comprising:

a disk I/O engine coupled to the bus interface (claim 5);

a device interface coupled to the disk I/O engine for interfacing the disk I/O engine with a disk drive, wherein the disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command from the processor, the disk I/O engine further configured to execute a disk transaction by processing the disk

transaction information from the bypass register coupled to the disk I/O engine (Claim 5).

Copending Application No. 12/005,745 does not teach the bridge component for implementing efficient disk I/O for the computer system, comprising:

a bus master controller coupled to the disk I/O engine;

a bypass register coupled to the bus master controller, wherein the bypass register is memory mapped, wherein the bypass register implements aggregation of disk transaction information from a host CPU by using a memory mapped data transfer;

an arbiter couple to the bus master controller and the disk I/O engine, to coordinate data transfers within the disk controller;

a chain memory coupled to the disk I/O engine for buffering a plurality of CPBs to extend a number of disk transactions scheduled for execution by the disk I/O engine; and

before completion of said start up, the disk start up command configured to hide a start latency of the disk drive.

Chisholm teaches a bridge component for implementing efficient disk I/O for a computer system, comprising:

a disk controller (Fig. 3, ref. 201, 203, 209, 213, 311) for executing disk transactions (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21), the disk controller further comprising:

a disk I/O engine (Fig. 3, ref. 209, 213) coupled to the bus interface (Fig. 3, ref. 109, 111) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine, wherein the bypass register is memory mapped and implements aggregation (e.g. aggregation via transfer to accumulate) of disk transaction information (e.g. command block with transaction information for data transferring) from a host CPU (Fig. 3, ref. 103) by using a memory mapped data transfer (e.g. memory mapped data transfer corresponding to the transferring of the command blocks via memory mapping by command block address to the host memory) (col. 5, l. 1 to col. 6, l. 21), wherein the register (Fig. 3, ref. 311) is memory mapped as the register comprises the command block address received from the host CPU for transferring of the command/data blocks (Fig. 3, ref. 301) (e.g. transaction information) (col. 5, ll. 25-34), wherein the command block address is mapped to where the corresponding command/data block is located in the host memory (Fig. 3, ref. 107) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a chain memory (e.g. section of the memory 203 storing the command blocks 304 of Fig. 3, wherein the memory section is the chain memory storing the chain of command blocks as the addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a plurality of command blocks (Fig. 3, ref. 304) to extend a number of disk transactions scheduled for execution by the disk I/O engine (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21); and

Winkler teaches a system and a method comprising:

a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) ([0013]), by combining the bus master controller with Copending Application No.

12/005,745 and Chisholm's bypass register and disk I/O engine, the resulting combination further teaches the bypass register which is coupled to the disk I/O engine is coupled to the bus master controller; and

an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller ([0013]), wherein the inclusion of the arbitration function into the disk controller would enable proper coordination of the data transferring for disk drive system such as RAID.

Wilcox teaches a system and a method comprising: causing the start up before completion of said start up, the start up command configured to hide a start latency of the disk drive (Fig. 7; col. 2, ll. 10-23; col. 3, ll. 40-62; col. 5, ll. 7-41; and col. 11, l. 38 to col. 12, l. 57), as the delay to for the start up of data transferring is hidden.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Chisholm's interfacing architecture, Winkler's bus master controller and arbitration, and Wilcox's start up into Copending Application No. 12/005,745's computer system for the benefit of increasing data transferring throughput by reducing the command block transfer overhead (Chisholm, col. 2, ll. 20-50 and col. 5, ll. 55-58), increasing the operation speed, as well as improving reliability and the efficiency in the transferring of data (Winkler, [0017]), ad reducing latency in the transferring of data to the disk drive (Wilcox, col. 1, ll. 19-23 and col. 2, ll. 51-53) to obtain the invention as specified in claim 8.

## II. ELECTION / RESTRICTIONS

9. Since applicant did not following the restriction requirement regarding the copending application 12/005,745, as the independent claims 1 and 5 of the copending application 12/005,745 only included the inventive features of the independent generic claims 1 and 8 in the instant parent application 10/725,663; therefore, the examiner is rejecting the instant application with the copending application 12/005,745 based on double patenting.

Additionally, the examiner recommend that the applicant to cancel the withdrawn claims 2-5, 9-11 and 14-20, as the claimed features of these withdrawn claims have been filed in the co-pending applications 12/005,745 and 12/005,816 respectively.

## III. REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 6, 8, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Chisholm et al. (US Patent 5,968,143), Winkler et al. (US Pub:. 2004/0024948) and Wilcox (US Patent 6,185,634).

11. As per claims 1, 8 and 21, AAPA teaches a computer system, comprising:

executing disk I/O transactions for the computer system (Specification, p. 2, l. 2 to p. 5, l. 4); and

a plurality of CPBs to extend a number of disk transactions (Specification, p. 2, l. 2 to p. 5, l. 4).

AAPA does not teach a disk controller and a bridge component for implementing efficient disk I/O for a computer system, comprising: a bus interface for interfacing … ; a disk controller for executing … : a disk I/O engine coupled to the bus interface; a bus master controller coupled to the disk I/O engine; a bypass register coupled to the bus master controller … ; an arbiter couple to the bus master controller … ; a chain memory coupled to the disk I/O engine … ; and a device interface coupled to the disk I/O engine … .

Chisholm teaches a disk controller and a bridge component for implementing efficient disk I/O for a computer system, comprising:

a bus interface (Fig. 3, ref. 109, 111) for interfacing with a processor (Fig. 1, ref. 103) and a system memory (Fig. 3, ref. 301) of the computer system (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a disk controller (Fig. 3, ref. 201, 203, 209, 213, 311) for executing disk transactions (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21), the disk controller further comprising:

a disk I/O engine (Fig. 3, ref. 209, 213) coupled to the bus interface (Fig. 3, ref. 109, 111) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine, wherein the bypass register is memory mapped and implements aggregation (e.g. aggregation via transfer to accumulate) of disk transaction information (e.g. command block with transaction information for data transferring) from a host CPU (Fig. 3, ref. 103) by using a memory mapped data transfer (e.g. memory mapped data transfer corresponding to the transferring of the command blocks via memory mapping by command block address to the host memory) (col. 5, l. 1 to col. 6, l. 21), wherein the register (Fig. 3, ref. 311) is memory mapped as the register comprises the command block address received from the host CPU for transferring of the command/data blocks (Fig. 3, ref. 301) (e.g. transaction information) (col. 5, ll. 25-34), wherein the command block address is mapped to where the corresponding command/data block is located in the host memory (Fig. 3, ref. 107) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a chain memory (e.g. section of the memory 203 storing the command blocks 304 of Fig. 3, wherein the memory section is the chain memory storing the chain of command blocks as the addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a plurality of command blocks (Fig. 3, ref. 304) to extend a number of disk transactions scheduled for execution by the disk I/O engine (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21); and

a device interface (Fig. 2, ref. 217) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for interfacing the disk I/O engine with a disk drive (e.g. SCSI RAID disk drives), wherein the disk I/O engine is configured to cause a start up of the disk drive

upon receiving a disk start up command (e.g. command transfer start signal) from the processor, the disk I/O engine further configured to execute a disk transaction by processing the disk transaction information (Fig. 3, ref. 304) from the bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21), as the command/data blocks are transferred to the memory mapped bypass register for implementing disk transaction and bypass the writing of a set of 8 bit registers in the disk controller as implemented in ATA disk drives.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Chisholm's interfacing architecture into AAPA's computer system for the benefit of increasing data transferring throughput by reducing the command block transfer overhead (Chisholm, col. 2, ll. 20-50 and col. 5, ll. 55-58) to obtain the invention as specified in claims 1, 8 and 21.

AAPA and Chisholm do not teach the disk controller and the bridge component for implementing efficient disk I/O for the computer system, comprising: a bus master controller coupled to the disk I/O engine; an arbiter couple to the bus master controller … ; and causing the start up before completion of said start up ….

Winkler teaches a system and a method comprising:

a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) ([0013]), by combining the bus master controller with AAPA and Chisholm's bypass register and disk I/O engine, the resulting combination further teaches the bypass

register which is coupled to the disk I/O engine is coupled to the bus master controller; and

an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller ([0013]), wherein the inclusion of the arbitration function into the disk controller would enable proper coordination of the data transferring for disk drive system such as RAID.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Winkler's bus master controller and arbitration into AAPA and Chisholm's disk controller for the benefit of increasing the operation speed, as well as improving reliability and the efficiency in the transferring of data (Winkler, [0017]) to obtain the invention as specified in claims 1, 8 and 21.

AAPA, Chisholm and Winkler do not teach the disk controller and the bridge component for implementing efficient disk I/O for the computer system, comprising causing the start up before completion of said start up ….

Wilcox teaches a system and a method comprising: causing the start up before completion of said start up, the start up command configured to hide a start latency of the disk drive (Fig. 7; col. 2, ll. 10-23; col. 3, ll. 40-62; col. 5, ll. 7-41; and col. 11, l. 38 to col. 12, l. 57), as the delay to for the start up of data transferring is hidden.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Wilcox's start up into AAPA, Chisholm and Winkler's disk controller for the benefit of reducing latency in the transferring of data to the disk drive

(Wilcox, col. 1, ll. 19-23 and col. 2, ll. 51-53) to obtain the invention as specified in claims 1, 8 and 21.

12. As per claims 6 and 12, AAPA, Chisholm, Winkler and Wilcox teach all the limitations of claims 1 and 8 as discussed above, where AAPA, Chisholm and Winkler further teach the disk controller further comprising: a CPB pointer buffer (Chisholm, command address queue 309 of Fig. 3) coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers (e.g. addresses pointing to where the command block are stored) to extend to a number of disk transactions scheduled for execution by the disk I/O engine, the CPB pointer buffers (Chisholm, Fig. 3, ref. 309) directly connected to the disk I/O engine (Chisholm, Fig. 3, ref. 209, 213) for control independent of the arbiter (AAPA, Specification, p. 2, l. 2 to p. 5, l. 4; Chisholm, Fig. 1-3; col. 4, l. 26 to col. 6, l. 21; and Winkler, [0013]).

## IV. CLOSING COMMENTS

### CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 16, 2010
/Chun-Kuan Lee/
Examiner, Art Unit 2181